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CAVIUM ADDS DSP FOR SMALL CELLS

Performance, Software Set Octeon Fusion Apart

By Joseph Byrne {10/10/11-01}

The first public hint that Cavium was interested in LTE technology, beyond supplying Octeon processors for infrastructure, came in January this year when the company acquired the assets of Wavesat, a vendor that had been sampling an LTE baseband chip for USB dongles and other user equipment since 2009. At the time of the acquisition, however, Cavium had already been working on its own LTE baseband—not for user equipment like dongles and handsets but for base stations.

The company disclosed details of the first chips from this design effort at the recent Linley Tech Processor Conference in San Jose. The aptly named Octeon Fusion merges Cavium's multicore Octeon processor with a new multicore baseband DSP. Supporting 64 and 256 users, respectively, the first Fusion processors, the CNF7120 and CNF7130, aim for the midrange and high end of the small-cell market, eschewing residential femtocells. A future chip, the CNF7280, will support even more users and deliver additional DSP performance, as Table 1 shows.

In pursuing this strategy, Cavium is aiming even higher than Texas Instruments, which also decided to forgo residential-scale devices to focus on femtocells for businesses (see *MPR 6/27/11*, "TI Tackles Small Base Stations"). The upstart also faces off against Freescale, which offers chips for both residential and enterprise femtocells and plans to scale up to larger base stations (see *MPR 2/21/11*, "Freescale Cues CPU-DSP Hybrid"). Undoubtedly as these and other companies flesh out their product lines, head-to-head match-ups will proliferate. Cavium diverges from these competitors by integrating more cores—four CPUs at 1.5GHz and six DSPs at 500MHz in the CNF7130, enabling its use in larger-scale base stations.

Cavium also provides a complete suite of Layer 1–3 software. The company collaborated with an undisclosed OEM to develop this stack. Using discrete Octeon processors and DSPs implemented in FPGAs as stand-ins for a finished Fusion processor, the two companies and a network operator ran the software through interoperability testing (IOT). Having such tight collaboration with an OEM indicates that Cavium, a newcomer to baseband processing, has already landed an initial win for Fusion. Shipments could ramp quickly owing to the completion of IOT, which is often a major source of headaches and delays for wireless chips and systems. The company must still, however, validate that the actual Fusion silicon, which will not sample until 1Q12, matches the function of the prototypes.

Fusion's powerful combination of high-performance hardware and production-ready software instantly puts Cavium on the map as a supplier of baseband processors for cellular base stations. All that the company needs now is for operators to begin deploying small cells—an action that has been delayed as these operators sort out the associated technical and financial challenges.

	CNF7120	CNF7130	CNF7280
Max LTE Users	64 active	256 active	>300 active
LTE (down/up)	100Mbps/75Mbps	150Mbps/150Mbps	300Mbps/300Mbps
Max 3G Users	32 active	128 active	>128 active
cnMIPS CPUs	2 @ 800MHz	4 @ 1.5GHz	6 @ 2.0GHz
DSP Cores	4 @ 400MHz	6 @ 500MHz	8 @ 1.0GHz
IC Process	40nm*	40nm*	28nm*
Package	31mm BGA-900	31mm BGA-900	31mm BGA-900
Samples	1Q12 (est)	1Q12 (est)	2H12 (est)

Table 1. Cavium's Octeon Fusion product line. These processors use multiple CPUs and DSPs to achieve high performance. (Source: Cavium, except *The Linley Group estimate)

Heterogeneous Multicore Takes Hold

Of the two sides to Fusion—CPU and DSP—the CPU side is familiar to students of Cavium's Octeon architecture (see *MPR 5/31/10,* "Cavium Pushes Octeon to 32 CPUs"). The key element is an original MIPS64-compatible CPU core that is replicated two to six times, depending on the Fusion model. The CPU is substantially similar to that used in Octeon II but operates at a faster rate (2.0GHz) owing, we believe, to implementation in a more advanced process. Although Octeon II is a 65nm design, recent Cavium chips use a 40nm process; we believe the company is also using this process for the CNF7120/CNF7130 design. Due to sample later and operating at this faster 2.0GHz rate, the CNF7280 is likely a 28nm design like the forthcoming Octeon III.

Octeon CPUs are comparatively simple designs, favoring economy of die area over wringing out more single-thread performance. At nine stages in the second generation, the pipeline is longer than that of Freescale's e500 but shorter than that of ARM CPUs used in competing chips. Further economy comes from supporting only two-way superscalar dispatch, which typically provides a 60% speed boost over scalar designs but only a moderate increase in die size. Targeting parallelizable networking applications, Cavium scales the performance of its processors by adding cores.

The CPUs' signature feature is their integrated encryption coprocessor, which uses the COP2 instruction space defined in the MIPS architecture. Other extensions accelerate packet-processing tasks, such as moving data among caches and performing bit manipulation. Absent are floating-point and SIMD units. An FPU is unlikely to be used in networking or even cellular applications. A SIMD unit, however, can be more efficient than a scalar ALU for scheduling users' transmissions in a base station—a fact that we believe contributed to Freescale bringing AltiVec back to its newer CPU designs (see *MPR 6/27/11*, "Freescale Amplifies QorIQ Family"). Supporting hundreds of users, Fusion is not lacking in scheduling horsepower.

As with other Octeon processors, Fusion includes numerous packet interfaces and accelerators. The most salient of these is a pair of Gigabit Ethernet ports and a unit for scheduling the dispatch of packets to the CPU. The Ethernet interfaces support IEEE 1588v2 and SyncE for transmitting timing information.

Figure 1 depicts a typical small-cell base station that employs Fusion. In this design, one Ethernet port connects to the backhaul network and another provides a management interface. If the backhaul link does not provide timing information via IEEE 1588 or SyncE, an optional GPS receiver can be connected. Complementing Fusion's support for 2×2 MIMO, an RF transceiver performs up/down conversion for two receive and two transmit channels.

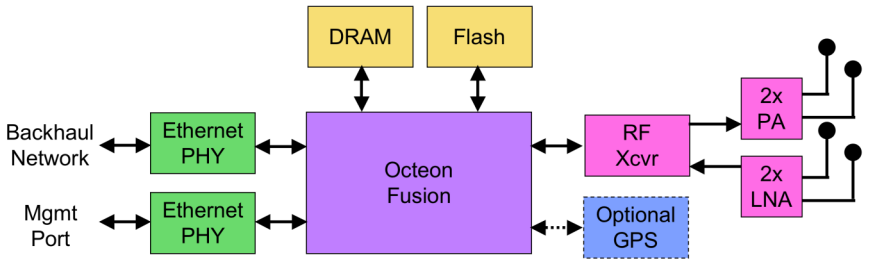

Figure 1. Block diagram of a base station using Octeon Fusion. Fusion obviates major digital logic chips in a small-cell base station.

Three Is Smaller Than One

Fusion's DSP side is all new. Here, too, Cavium's emphasis on parallel processing and area-efficient cores is evident. The CNF7130 has a heterogeneous mixture of six DSPs. Three cnMBP cores handle symbol processing (OFDM algorithms such as channel estimation, equalization, and demodulation): one for the downlink and two for the uplink. Optimized for soft-bit processing, two cnSBP cores handle tasks such as data interleaving. Yet another architecture, the sixth DSP offloads control functions. The CNF7120 cuts the design to four DSPs: two for symbol processing, one for soft-bit processing, and one for baseband control. The CNF7280 adds two DSPs and accelerators and operates at a higher clock rate to enable greater over-the-air bandwidth and support for wireless backhaul.

Numerous engines supplement these DSPs to accelerate WCDMA (3G) and OFDM (4G) functions such as Fourier transforms, WCDMA chip-rate processing, encoding/decoding data as symbols, turbo coding, and Viterbi coding. Other accelerators perform pulse shaping and peak-to-average power reduction. These are digital front-end (DFE) functions, performed in a separate chip in many systems, that improve the performance of a base station's transmitter. The engines are local to each pair of DSPs. For example, the DFE engines are integrated with the DSPs handling the downlink, and the turbo and Viterbi engines are integrated with the soft-bit DSPs.

Cavium claims that in total, three of its purpose-built DSPs consume less die area than one TI C66x or Freescale StarCore 3850 DSP. These competing DSPs are designed for use throughout TI's and Freescale's product lines. The C66x, moreover, also supports floating-point computations. Thus, these DSPs are conceivably less area-efficient than cores developed specifically for baseband processing.

Although CPU performance determines the number of users a base-station processor can support owing to the computational load of scheduling transmissions, DSP performance determines link rates. The fastest LTE rate commonly discussed for user equipment (UE) is Category 5, which specifies

a peak of 300Mbps for the downlink (base station to user) and 75Mbps for the uplink. Category 4 is significantly slower, halving the downlink to 150Mbps and reducing the uplink to 50Mbps. The two categories use the same modulation scheme and assume 20MHz channels, but Category 5 transmits four spatial streams in the downlink (4×4 MIMO) compared with two streams (2×2 MIMO) for Category 4. Category 3 is similar to Category 4 but specifies less error correction, reducing the downlink to 100Mbps.

Cavium rates the CNF7120 at 100Mbps down and 75Mbps up for 64 users. This level of performance is sufficient to support Category 3 UE, leaving additional DSP headroom on the uplink for interference cancellation and other techniques to improve communications robustness. The same techniques can be used with the CNF7130; that chip has more than enough performance to support 150Mbps downlinks and 256 users. The surplus processing capacity could power multiuser MIMO, a technology that extends the concept of simultaneous transmission of different streams in the same band. Cavium rates the CNF7280, due to sample much later than the CNF7120/CNF7130 pair, at more than 300Mbps up and 300Mbps down, enabling Category 5 operation and providing DSP headroom for wireless backhaul and coordination among neighboring cells, as well as interference cancellation and multiuser MIMO.

An important factor in Fusion's performance and power efficiency is the architecture by which the DSPs access and share memory. Each pair of DSPs and accelerators has a large memory shared by these major blocks and connected to the corresponding memory in adjacent subsystems, as Figure 2 shows. A 128-bit bus provides single-cycle access to this memory faster and more deterministically than if Fusion had used a cache. Although Cavium began the Fusion project before acquiring Wavesat, Wavesat's use of this shared-memory architecture influenced the final Fusion design.

For communicating with distant blocks on chip or with off-chip memory, the DSP subsystems connect to Fusion's main bus. A separate interface connects the subsystems to a base station's RF unit. To facilitate system design, Fusion supports JESD 207P and CPRI interfaces.

The provenance and architecture of the DSPs is unknown. We speculate that Cavium bases the DSPs on cores from Tensilica, which has focused heavily on adapting its Xtensa chip to LTE baseband processing. Tensilica offers the ConnX baseband engine (BBE16), which can perform sixteen 18×18-bit multiply-accumulate operations per cycle (see *MPR 8/10/09,* "Tensilica Plays Baseband"). The company has also developed other adaptations of Xtensa for soft-bit processing. Chip designers can modify these cores, as well as the BBE16, or use them as inspiration for their own customization of Xtensa. Wavesat has successfully used Tensilica cores in its LTE modem.

Forgoing Four-User Femtocells

Slated to sample in early 2012, the CNF7130 and CNF7120 appear to be one to two quarters behind small-cell processors from TI and Freescale. This small gap puts Cavium in the scrum for new LTE designs. LTE deployments are well underway worldwide as operators upgrade their macrocells. Most of these operators agree that numerous smaller base stations must eventually be deployed to deliver high-bandwidth service to large numbers of simultaneous users. The open questions are how pervasive these small systems will be and when their shipments will ramp.

Initial enthusiasm for femtocells centered on residential systems capable of serving a handful of users. Their principal value to operators is the retention of customers frustrated by poor voice coverage. Over the past few years, the industry has shifted emphasis to offloading data and deploying small stations—variously called femtocells, picocells, and microcells depending loosely on their user capacity—outdoors and in the enterprise. These small cells have more capacity: 32 or more users compared with 4 for residential femtocells. *Small* describes their cost better than their capabilities. They must be inexpensive to acquire, install, and operate. Although the amount of data shuttled over the air is skyrocketing, carriers' revenues are only inching upward. Their budgets for capital expenditures (capex) are creeping upward even slower.

Targeting designs supporting no fewer than 32 users, Cavium is deliberately foregoing the residential market. There is logic to this approach. Home users may be better served by 3G-only femtocells with data offloaded to Wi-Fi. If so, companies such as Broadcom and Qualcomm, which both have 3G femtocell chips and successful Wi-Fi businesses, are in a better position to serve that market. Unit volumes may be substantial for residential systems, but profit margins will be slim. Moreover, Taiwanese ODMs

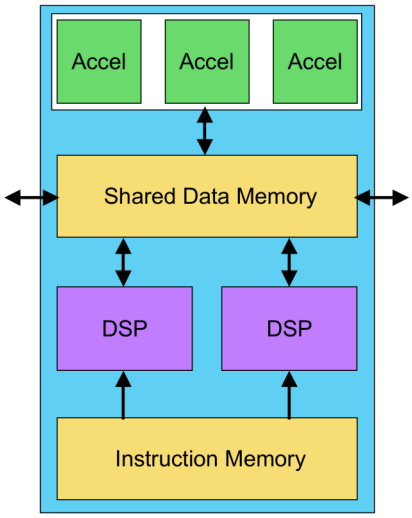

Figure 2. Memory architecture of Octeon Fusion's DSP subsystem. Fast connections to shared memory minimize stalling in the DSP pipeline and improve power efficiency.

Price and Availability

The Octeon Fusion CNF7120 and CNF7130 are due to sample in early 2012. Pricing has yet to be disclosed. For more information, download Cavium's presentation from the Linley Tech Processor Conference by clicking to *www.linleygroup.com/events/proceedings.php?num=10*

are likely to become the main suppliers of residential femtocells (displacing the niche companies dominating the market today), not the Tier One OEMs that Cavium counts among its leading Octeon customers.

Coming in at the high end also clearly defines Fusion's position in the competitive landscape. The Freescale Qonverge PSC9132 and TI Keystone TCI6612 are similar to the CNF7130, as Table 2 shows.

The PSC9132 and CNF7130 support comparable data rates and have other similarities, but the two chips target different system classes. Supporting fewer users and packing only two 1.0GHz CPUs compared with four CPUs at 1.5GHz, the PSC9132 is better for enterprise femtocells, whereas the CNF7130 is better for microcells serving the general public. Not surprisingly, Fusion's added performance comes at the cost of higher power consumption. Cavium is coy about specifics, hinting informally that the 10W rating is exceptionally conservative, but the CNF7130 is unlikely to meet Freescale's 6W maximum.

Both have standard antenna interfaces and a complete Layer 1–3 stack. Cavium has the advantage of IOT validation of its stack; Freescale has the advantage of running its stack on a mature DSP architecture. Whereas Cavium worked with an OEM to develop its software, Freescale worked with software vendors. Freescale also has the advantages of having begun sampling its small-cell processor and having an installed customer base for its DSP architecture. The company has withheld details of its roadmap, but it has stated that future products will support more users and have higher performance, creating a bigger overlap with Cavium's lineup. The standard interfaces, approach to software, and simultaneous multimode operation will likely carry through to new chips.

The Keystone TCI6614 has a wimpy CPU subsystem: a single ARM Cortex-A8. Unlike other designs, however, the TI chip uses its DSPs for scheduling transmissions. This approach reduces the DSP cycles available for other tasks, like actual signal processing. The processor's Category 5 rating assumes only 20 users and 500-byte packets. TI conveniently assumes that customers will use its RF chips and thus does not provide a standard interface. Power consumption is higher than that of Fusion, and because it omits a turnkey Layer 1–3 stack, TI does not match Cavium in software availability. The TCI6614, however, may be more attractive to OEMs among TI's broad customer base that have their own software.

Other alternatives to Fusion include the Mindspeed Transcede 4000 and the DesignArt Networks DAN3300. Like Fusion, Transcede has numerous processor cores: six ARM Cortex-A9 CPUs, 10 Ceva-X1641 DSPs, and 10 "application processor" engines. This processor targets three-sector macro base stations. Critically, Mindspeed does not offer a complete software stack. The DAN3300 has four ARM9 CPUs supplemented by six custom Xtensa cores for Layer 2–3 processing plus three custom Xtensas for signal processing. It supports 128 active users and up to 4×4 MIMO configurations but does not come with a turnkey Layer 1–3 software stack.

Going In When the Going Is Good

Mobile infrastructure is now a hot target market for many communications-IC suppliers. One of the few areas where carriers are investing, this industry is undergoing several changes. Foremost among these is the transition to LTE and the concomitant interest in using many small base stations to supplement large macrocells. Both changes open the market to new chip suppliers, such as Cavium. The limited scope of small cells compared with a macro station enables a single chip to integrate all processing functions; moreover, operators' limited capex budget demands the cost savings that such integration enables.

Cavium is thus entering the market at an opportune moment and with what appears to be a powerful chip family. Its decisive strength may not be its hardware but instead its software. Not only does Cavium provide a Layer 1–3 stack, but the company and its co-developer have run

	Cavium Octeon Fusion CNF7130	Freescale Qonverge PSC9132	Texas Instruments Keystone TCI6614
CPU Cores	4×cnMIPS @ 1.5GHz	2×Power e500 @ 1.0GHz	1×ARM Cortex-A8 @ 1.2 GHz
DSP Cores	3×cnMBP + 2× cnSBP + 1×control @ 500MHz	2×StarCore 3850 @ 1.0GHz	4×C66x @ 1.2GHz
LTE (down/up)	150Mbps/150Mbps	150Mbps/75Mbps	300Mbps/150Mbps
Max LTE Users	256 users	64 users	128 users
Ethernet	2×GbE w/ 1588	2×GbE w/ 1588	2×GbE w/ 1588
RF Interface	JESD207, 12-bit I/Q	JESD207, CPRI	Proprietary
Vendor-Supplied Turnkey Software	Layer 1–3 (IOT validated)	Layer 1–3	Layer 1
Power (max)	<10W	6W	14W*
IC Process	40nm*	45nm	40nm
Samples	1Q12 (est)	Aug 2011	Oct 2011 (est)

Table 2. Comparison of Octeon Fusion and competitors. TI's Keystone has the highest stated data rates, but performance depends on the number of users. Freescale's Qonverge has the best power dissipation and is already sampling. The Fusion CNF7130 supports the most users and has IOT-validated software. (Source: vendors, except *The Linley Group estimate.)

the stack through interoperability testing. For customers seeking a turnkey solution, such software accelerates their time to market—and Cavium's time to revenue.

How quickly Fusion customers get to market depends on the thoroughness of this testing (other OEMs and mobile operators will run their own tests) and how quickly Cavium can complete and validate the actual Fusion chip, which incorporates multiple new DSP architectures. The company's Octeon processors have already established a presence in mobile infrastructure. Despite being a newcomer to signal processing, Cavium is well armed to fight competitors (such as Freescale, Qualcomm, and TI) that have been in the cellular business for decades. ♦